PAPER 14 – A SPACE VECTOR PULSE WIDTH MODULATED THREE PHASE INVERTER FOR AN IMPROVED SOLID-STATE TRANSFORMER DESIGN

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ABSTRACT
A Space Vector Pulse Width Modulation (SVPWM) technique is used for the implementation of a three phase DC-AC Voltage Source Converter (VSC). The VSC is used in design of an improved Solid-State Transformer (SST). Consequently, this paper discusses concept and operation of SVPWM as well as implementation of the technique to achieve a desired objective. VSC has been used to enable supply of variable voltages and frequency to AC drives and other areas of applications in the electric network. Several forms Pulse Width Modulation (PWM) Techniques to obtain variable voltage and frequency exist. Two of these PWM techniques are commonly used in the implementation of the VSC: SVPWM and Carrier-based PWM. Trend of use of SVPWM in the design of VSC is on increase due to its better utilization of DC bus and easier digital realization. Therefore, in this paper concept and implementation of SVPWM for VSC have been elucidated with the aid of MATLAB/Simulink environment. An LCL filter has been used in the design with the view to further mitigate harmonics. Performance of the VSC is evaluated in terms of Total Harmonic Distortion (THD).
KEYWORDS: *THD, SST SVPWM, VSC, LCL filter.*

1. INTRODUCTION

Voltage Source Converters (VSCs) are not mass-produced product. Therefore, they should be specifically designed for the applications they are used for. A VSC has been employing the use of Space Vector Pulse Width Modulation (SVPWM) scheme in its design this is to enable obtaining variable voltages and frequency for use in AC drives and other relevant areas of application. In this paper, a VSC is designed for implementation of an improved Solid-State Transformer (SST). SST has been investigated in recent years to either replace or work hand-in-hand with the conventional Low Frequency Transformer (LFT) (Ismail et al., 2022; Nondy & Nondy, 2021; Saju et al., 2020; Zhang et al., 2019). This is largely due to some advantages the SST posses relative to the LFT (Abu-Siada et al., 2018; Hannan et al., 2020; Londero et al., 2019; Mollik et al., 2022; Saju et al., 2020). These advantages include: It corrects Power Factor (PF); it can be used in both AC and DC systems; it controls both active and reactive power; it enables online communication in the event of fault and controls it etc. (Shafei et al., 2019; Tahir et al., 2019; Umar et al., 2020, 2021; Vaca-Urbano et al., 2020). However, the SST suffers some draw-backs which are: Less efficiency and reliability while compared to the LFT (Umar et al., 2020). In order to enhance efficiency of SST a designed SST is improved. To improve the SST, a SVPWM and an LCL filter are used in its design. The SVPWM is used particularly in the design of the DC-AC converter at the output stage of the SST. Consequently, the converter performance has greatly improved due to reduction of the THD and hence improves the performance of the SST. This paper describes VSC based on SVPWM; it further discusses THD obtained from the VSC. Schematic of SST is as shown in Fig.1.

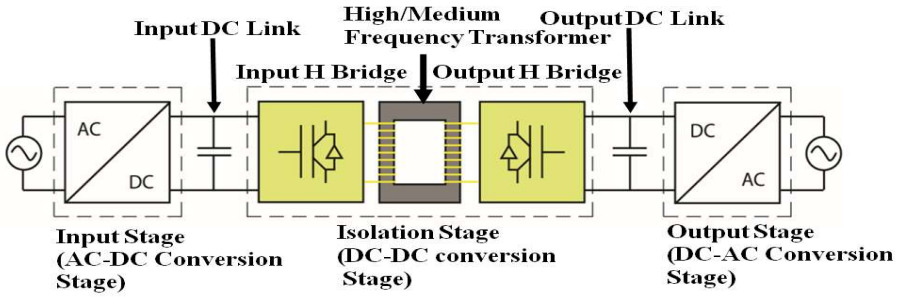


Fig. 1: Schematic of SST (Gajowik et al., 2017)

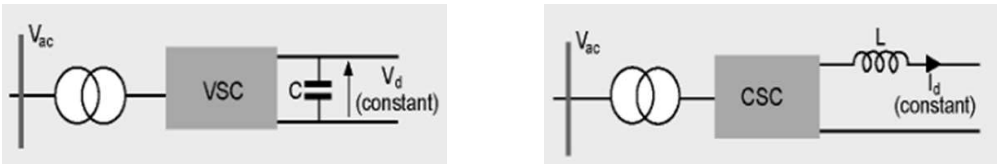
2. THEORETICAL ANALYSIS

2.1 Voltage source and current source converters

Active rectifiers employing use of VSC or CSC stand advantage both for traditional solutions such as the thyristor and for newer ones such as a chopper, due to the following (Banumathy & Veeraraghavalu, 2018):

i. Reduced number of power devices
ii. Capability of grid current control
iii. power factor correction

Voltage-sourced converter is a self-commuted converter that generates ac voltage from a dc voltage. VSC is often referred to as an inverter, even though it has the capable of bidirectional power flow. With a VSC, frequency of the output voltage, phase angle, and the magnitude can be controlled (Khan et al., 2021). In this type of converters the dc side voltage always has one polarity, and the power flow reversal takes place through reversal of dc current polarity. On DC side the voltage is supported by a capacitor. This capacitor should be capable to handle a sustained charge/discharge current that accompanies the switching sequence of the converter valves and shifts in phase angle of the switching valves without significant change in the dc voltage. The VSC connects HVAC and HVDC systems using devices suitable for high power electronic applications, such as MOSFETs and IGBTs (Khan et al., 2016). On the other hand in the CSC an inductor maintains the DC current constant. Schematic of VSC and CSC is as shown in Fig. 2.



(i) VSC (ii) CSC

Fig. 2: Schematics of (i) VSC and (ii) CSC

The use of the VSC in the design of the converter is due to its: (i) higher Voltage handling capability, (ii) High power rating, (iii) Better output voltage waveform, (iv) and less electromagnetic interference (Taylor et al., 2013).

VSC is usually connected to the power system at th Point of Common Coupling (PCC) through phase reactors, which also serve as filter inductors to further mitigate harmonics (Nandhini & Sivaprakasam, 2020).

2.2 Principle of SVPWM

A three-phase system can be represented by two-phase system. The two-phase quantities are referred to as vector. Vectors are defined in a complex plane since they allow to use the property of vectorial rotation. The space vector modulation is meant to be a three-phase sinusoidal waveform with respect to time on the three axes that are displaced in time with respect to each other by 120° yielding a constant amplitude space vector that rotates at a constant speed. In the case of SVPWM technique, the two-level DC-AC converter contains two zero vectors and six active vectors to generate the reference voltage which gets sampled once for every sub-cycle T_s. The SVPWM employs the switching sequence which divides the zero vector time equally for the two zero states in every sub-cycle. The maximum control voltage, V_c obtained using SVPWM is given by the expression

$$V_c = \frac{V_{DC}}{\sqrt{3}} \tag{1}$$

Reference voltage V_{REF} in SVPWM is given as follows:

$$V_{REF} = \sqrt{V_d^2 + V_q^2} \tag{2}$$

Where the two-phase quantities, V_d and V_q in (2) are given as in the following expressions respectively.

$$V_d = \frac{2}{3}\left[V_{an} - {}^1\!/_2\,(V_{bn} - V_{cn})\right] \tag{3}$$

$$V_q = \frac{2}{3}\left[\frac{\sqrt{3}}{2}(V_{bn} - V_{cn})\right] \quad (4)$$

The angle between the two-phase quantities is calculated using the expression:

$$\theta = tan\sqrt{V_d / V_q} \quad (5)$$

In SVPWM, the reference vector V_{REF} is synthesized by two active vectors and two zero vectors as shown Fig. 7. The Fig. 7 shows the voltage vectors of two-level DC-AC converter with six sectors 1 to 6. For example in Sector I, V_{REF} is realized by applying vector V_1' for an appropriate duration of T_1, vector V_2' for an appropriate duration of T_2 and V_0 for remaining duration in a sub-cycle of T_s, based on volt-second balance principle.

$$V_{REF}T_s = V_1T_1 + V_2T_2 + V_0T_0 \quad (6)$$

$$T_s = T_1 + T_2 + T_0 \quad (7)$$

Where,
VREF is reference vector, Ts is duration of sub cycle, T1 and T2 are dwell times active vectors and T0 is dwell time of zero vectors.

The dwell times T0, T1 and T2 are respectively calculated using the expressions,

$$T_0 = T_s - (T_1 + T_2) \quad (8)$$

$$T_1 = \frac{V_{REF}}{V_{DC}} \frac{Sin(60-\theta)}{Sin60} T_s \quad (9)$$

$$T_2 = \frac{V_{REF}}{V_{DC}} Sin \frac{\theta}{Sin(60)} T_s \quad (10)$$

2.3 LCL filter

An LCL filter is used in the design of the DC-AC converter to mitigate harmonics. The use of LCL filters becomes attractive due to their reduced component dimensions. The parameters of the designed improved SST in which the DC-AC converter is used are as shown in Table 2.

Table 2: Parameters specifications for the Designed improved SST (Tahir et al., 2019)

SNo	parameter	Value
1	Rating, S	200kVA
2	Input AC voltage, V_{1RMS}	11kV
3	Output AC voltage, V_{2RMS}	Variable
4	Output DC voltage, V_{2DC}	500V
5	Grid Frequency (F_o)	50Hz

Parameters of the filter are calculated as follows: The capacitance of the filter capacitor, C_f was calculated to be 46mF using the expression (Dursun & Dosoglu, 2018) :

$$C_{f2} = \frac{0.05 \,.\, P_0}{V_{1phRMS} \,.\, \omega_g} \quad (11)$$

Unity power factor was achieved therefore, Real power (P) = Apparent power (S). P_o which was a per phase power output of the SST was obtained by dividing the rated power of the SST in Table 3.1 by three (3). Also the phase

voltage V_{ph} was obtained by dividing V_{1RMS} in Table 2 by square root of 3. ω_g is the angular frequency at the grid side given as:

$$\omega_g = 2\pi F_o \tag{12}$$

Where F_o is the grid frequency.

Switching frequency, F_{sw} was selected to be 25kH. The resonance frequency which is the natural frequency where a medium vibrates at the highest amplitude denoted by 'F_r' was calculated by dividing the F_{sw} by 10. F_r was obtained to be 2.5 kHz.

The phase grid current i_{gph} was calculated to be 10.49A using the expression:

$$i_{gphRMS} = \frac{P_o}{V_{1phRMS}} \tag{13}$$

Peak I_{gph} that is $i_{gphp}$was obtained by multiplying I_{gphRMS} by square root of 2. It was obtained to be 14.84A.

The load resistance, R_L was calculated to be 605.21Ω by substituting V_{1php} and i_{gphp} in the following expression.

$$R_L = \frac{V_{1php}}{i_{gphp}} \tag{14}$$

Therefore, R_L value of 700Ω was considered for the design.

The $i_{gphp\ (sw)}$ that is the i_{gphp} during switching was calculated by multiplying i_{gphp} by the allowable percentage of 0.3 (0.3%). $i_{gphp\ (sw)}$ was calculated to be 0.044A.

The phase input voltage during switching [$V_{1phRMS\ (sw)}$] was calculated to be 5.72kV by multiplying V_{1phRMS} by 90% allowable voltage during switching.

Minimum inductance of the filter inductor (L_{min}) was calculated using the expression (Dursun & Dosoglu, 2018):

$$L_{min} = \frac{V_{1phRMS(sw)}}{i_{gphp\ (sw)} \cdot \omega_{sw}\ (1-\frac{\omega_r^2}{\omega_{sw}^2})} \tag{15}$$

ω_{sw} and ω_r were calculated as 157. 08 kHz and 15.71 kHz respectively using the expressions:

$$\omega_{sw} = 2\pi F_{sw} \tag{16}$$

$$\omega_r = 2\pi F_r \tag{17}$$

The L_{min} was obtained to be 0.84H. Therefore, $L_1 = L_2 = L_{min}/2$ which was equal to 420mH. Therefore, 500mH was considered for the design of the converter.

The maximum voltage drop at the filter inductor V_{Lmax} was calculated by multiplying V_{1php} by 20%. V_{Lmax} was obtained as 1796.29V.

The Quality factor, Q of the filter was calculated using the expression:

$$Q = R_L\sqrt{\frac{C}{L}} \tag{18}$$

However, because the designed filter was an LCL filter the resultant inductance (L_r) of the filter was calculated using the expression:

$$L_r = \frac{L_1^2}{2L_1} \tag{19}$$

L_r was calculated to be 0.297H. 300mH was used. And L was equal to L_r in all the related equations.

Therefore, the Quality factor, Q_o was obtained to be 6460.70. The Damping factor ξ_o was calculated to be 7.73 using the following expression.

$$\xi_o = \frac{1}{2Q} \tag{20}$$

The cut-off frequency was calculated to be 51.93Hz. The obtained parameters of the filter were as indicated in Table 3. Schematic of the designed LCL filter was as shown in Fig. 3.

Table 3: Parameters of the Designed three phase input LCL Filter

SN	Parameter	Calculated value
1	Load resistance, R_L	700Ω
2	Capacitance, C_{f2}	23mF
3	Inductance, L_{o1}	500mH
4	Cut-off frequency, F_{co}	51.93Hz
5	Quality factor, Q_o	6460.70
6	Damping factor, ξ_o	7.73

Designed LCL filter schematic of per phase model is as shown in Fig. 3.

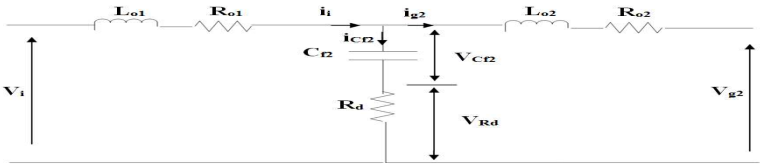


Fig. 3: Designed LCL filter per-phase model

Considering Fig. 3, the per phase state space model of the designed LCL is derived as follows:

$$\begin{cases} \dfrac{d_{i_i}}{dt} = \dfrac{1}{L_{o1}}\left[v_i - v_{c_{f2}} - R_d\left(i_i - i_{g2}\right) - R_{o1}i_i\right] \\ \dfrac{d_{g2}}{dt} = \dfrac{1}{L_{o2}}\left[v_{v_{c_{f2}}} + R_d\left(i_i - i_{g2}\right) - v_{g2} - R_{o2}i_{g2}\right] \\ \dfrac{d_{v_{c_{f2}}}}{dt} = \dfrac{i_i - i_{g2}}{C_{f2}} \end{cases} \tag{21}$$

Therefore, the state space equation of the designed three phase output LCL filter per-phase model is as follows:

$$\begin{bmatrix} \frac{d_{i_i}}{dt} \\ \frac{d_{i_{g2}}}{dt} \\ \frac{d_{v_{c_{f2}}}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{o1}+R_d}{L_{o1}} & -\frac{R_d}{L_{o1}} & -\frac{1}{L_{o1}} \\ \frac{R_d}{L_{o2}} & -\frac{R_{o2}+R_d}{L_{o2}} & \frac{1}{L_{o2}} \\ \frac{1}{C_{f2}} & -\frac{1}{C_{f2}} & 0 \end{bmatrix} \begin{bmatrix} i_i \\ i_{g2} \\ v_{c_{f2}} \end{bmatrix} + \begin{bmatrix} \frac{1}{L_{o1}} & 0 \\ 0 & -\frac{1}{L_{o2}} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} v_i \\ v_{g2} \end{bmatrix} \tag{22}$$

Therefore, the state space equation of designed three phase LCL filter model is derived considering Fig.4 as follows:

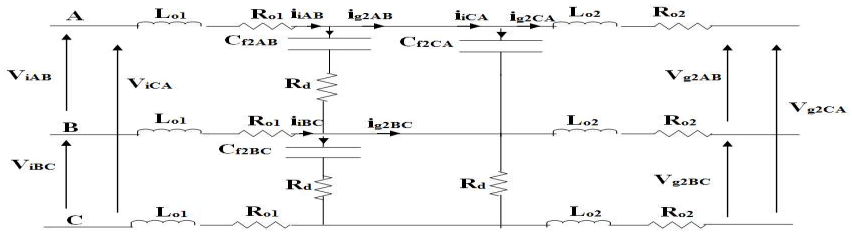


Fig. 4: Designed three phase output LCL filter model

where $i_{g2} = [i_{g2AB}\ i_{g2BC}\ i_{g2CA}]^T$, $v_{g2} = [v_{g2AB}\ v_{g2BC}\ v_{g2CA}]^T$, $v_{cf2} = [V_{Cf2AB}\ V_{Cf2BC}\ V_{Cf2CA}]^T$, $i_i = [i_{iAB}\ i_{iBC}\ i_{iCA}]^T$, and $v_i = [V_{iAB}\ V_{iBC}\ V_{iCA}]^T$.

$$\begin{bmatrix} \frac{di_i}{dt} \\ \frac{di_{g2}}{dt} \\ \frac{dv_{cf2}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{o1}+R_d}{L_{o1}} I_{3X3} & -\frac{R_d}{L_{o1}} I_{3X3} & -\frac{1}{L_{o1}} I_{3X3} \\ \frac{R_d}{L_{o2}} I_{3X3} & -\frac{R_{o2}+R_d}{L_{o2}} I_{3X3} & \frac{1}{L_{o2}} I_{3X3} \\ \frac{1}{3C_{f2}} I_{3X3} & -\frac{1}{3C_{f2}} I_{3X3} & 0I_{3X3} \end{bmatrix}_{9X9} \begin{bmatrix} i_i \\ i_{g2} \\ v_{cf2} \end{bmatrix}_{9X1} + \begin{bmatrix} \frac{1}{L_{o1}} I_{3X3} \\ -\frac{1}{L_{o2}} I_{3X3} \\ 0_{3X3} \end{bmatrix}_{9X1} \begin{bmatrix} v_{g2} \\ v_i \end{bmatrix}_{9X1} \quad (23)$$

Simulink model of the designed three phase DC-AC converter is as shown in Fig. 5. Schematic of the designed DC-AC converter model is as shown in Fig. 6.

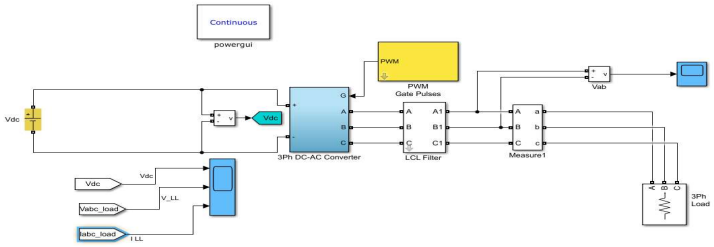


Fig. 5: Simulink model of the designed DC-AC converter

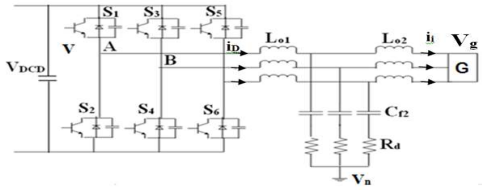


Fig. 6: Schematic of the designed Three Phase DC-AC converter for analysis

Vector representation of the SVPWM is presented in Fig.7. The active states divide equally the space vector plane into six sectors as shown in Fig. 7. The switching states of the six active and two null vectors are as presented in Table 4.

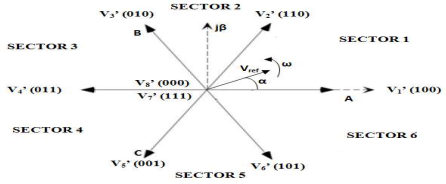


Fig. 7: Vector representation of the SVPWM

Table 4: Switching states corresponding to space vectors

SN	Switching gate			Line-Neutral Voltage			Line-Line Voltage		
	A	B	C	V_{AN}	V_{BN}	V_{CN}	V_{AB}	V_{BC}	V_{CA}
1	0	0	0	0	0	0	0	0	0
2	1	0	0	$2/3V_{DC}$	$-1/3V_{DC}$	$-2/3V_{DC}$	V_{DC}	0	$-V_{DC}$
3	1	1	0	$1/3V_{DC}$	$1/3V_{DC}$	$-2/3V_{DC}$	0	V_{DC}	$-V_{DC}$
4	0	1	0	$-1/3V_{DC}$	$2/3V_{DC}$	$-1/3V_{DC}$	$-V_{DC}$	V_{DC}	0
5	0	1	1	$-2/3V_{DC}$	$1/3V_{DC}$	$1/3V_{DC}$	$-V_{DC}$	0	V_{DC}

6	0	0	1	-1/3V_{DC}	-1/3V_{DC}	2/3V_{DC}	0	-V_{DC}	V_{DC}
7	1	0	1	1/3V_{DC}	-2/3V_{DC}	1/3V_{DC}	V_{DC}	-V_{DC}	0
8	1	1	1	0	0	0	0	0	0

A rotating space vector V (t) in complex rotation is given by:

$$V(t) = \frac{2}{3}\left[V_A + V_B e^{j\left(\frac{2}{3}\right)\pi} + V_C e^{-j\left(\frac{2}{3}\right)\pi}\right] \quad (24)$$

Therefore, considering (14), the output phase voltage in switching state 100 is given as:

$$V_A(t) = \frac{2}{3}V_{DC} \quad (25)$$

$$V_B(t) = -\frac{1}{3}V_{DC} \quad (26)$$

$$U_C(t) = -\frac{1}{3}V_{DC} \quad (27)$$

Therefore:

$$V_1' = \frac{2}{3}\left[\frac{2}{3}V_{DC} - \frac{1}{3}V_{DC}e^{j\left(\frac{2}{3}\right)\pi} - \frac{1}{3}V_{DC}e^{-j\left(\frac{2}{3}\right)\pi}\right] \quad (28)$$

$$\Rightarrow V_1' = \frac{2}{3}V_{DC}e^{j0} = V_1' = \frac{2}{3}V_{DC} \quad (29)$$

Therefore, for all the six active vectors, the voltage is calculated using the expression:

$$V_N' = \frac{2}{3}V_{DC}e^{j(N-1)\frac{\pi}{3}} \quad (30)$$

For N = 1, 2, 3…6

Considering Fig. 6 the State space equation of the designed DC-AC converter was derived as thus,

$$\begin{cases} L_{o1}\frac{di_D}{dt} = V_{DCD} + V - V_{C_{f2}} - V_{R_d} - V_n \\ C_{f2}\frac{dV_{C_{f2}}}{dt} = i_D - i_g \\ L_{o2}\frac{di_g}{dt} = V_{C_{f2}} + V_{R_d} + (V_n - V'_n)1 - V_g \end{cases} \quad (31)$$

Where,

i_D, i_g, V_{Cf2}, and V_g, were DC-AC converter side current voltage, grid side current vector, outfut LCL filter capacitor voltage vector and grid voltage vector respectively and were given as:

$i_D = [i_A \quad i_B \quad i_C]$, $i_g = [i_{gA} \quad i_{gB} \quad i_{bC}]$, $V_{cf2} = V_{cf2A} \quad V_{cf2B} \quad V_{cf2C}]$ and $V_g = [V_{gA} \quad V_{gB} \quad V_{gC}]$.

Also,

V was the Control signal vector given as

$V = [V_A \quad V_B \quad V_C]$, V_n and V'_n were voltages at the neutral points and 1 was a column vector defined as [1 1 1].

Considering (31), the neutral point voltages were derived as thus,

$$V_n = \frac{V_{DCD}}{3}(V_A + V_B + V_C) - \frac{1}{3}\left(V_{Cf2A} + V_{Cf2B} + V_{Cf2C}\right) \quad (32)$$

$$V_n' = \frac{V_{DCD}}{3}(V_A + V_B + V_C) - \frac{1}{3}\left(V_{gA} + V_{gB} + V_{gC}\right) \quad (33)$$

Assuming that the grid voltages are balanced (i.e $V_{Cf2A} + V_{Cf2B} + V_{Cf2C} = 0$ and $V_{gA} + V_{gB} + V_{gC} = 0$), therefore, the expression for the neutral voltages were reduced to:

$$V_n = V_n' = \frac{V_{DCD}}{3}(V_A + V_B + V_C) \tag{34}$$

The expression for the three phase DC-AC converter became:

$$\begin{cases} L_{o1}\frac{di_D}{dt} = V_{DCD} + V - V_{C_{f2}} - V_{R_d} - V_n \\ C_{f2}\frac{dV_{C_{f2}}}{dt} = i_D - i_g \\ L_{o2}\frac{di_g}{dt} = V_{C_{f2}} + V_{R_d} - V_g \end{cases} \tag{35}$$

(35) can be re-written as a discrete state-space model. Thus,

$$x_i(k+1) = Ax_i(k) + Bu_1(k) + DV_1(k) + EV_n(k) \tag{36}$$

$$y_i(k) = Hx_i(k) \tag{37}$$

Where,

$x_i(k) = (i_{Ai} \quad u_i \quad i_{gi})$ is the state- space vector, H is the output matrix defined as H = (1 0 0)

3. MATERIALS AND METHODS/METHODOLOGY/EXPERIMENTAL PROCEDURE

MATLAB 2022Ra environment was used in the design of the DC-AC Simulink model. The FFT analysis was carried out using the same software. The DC-AC was design to compose of LCL filter which was mathematical designed as shown earlier, the Converter itself. IGBTs were used to in the design of the active converter. SVPWM was used to control the signal supplied to the power electronics switches to align with the input and output signals requirements.

4. RESULTS AND DISCUSSION

The Simulink model of the designed three phase DC-AC converter is simulated on MATLAB environment.
The line to line output voltage of the DC-AC converter was 545V as presented in Fig. 8. Also, phase output voltage of the designed DC-AC converter was found to be 324V as shown in Fig. 9. In both waveforms, nearly pure sinusoidal waveforms were achieved.

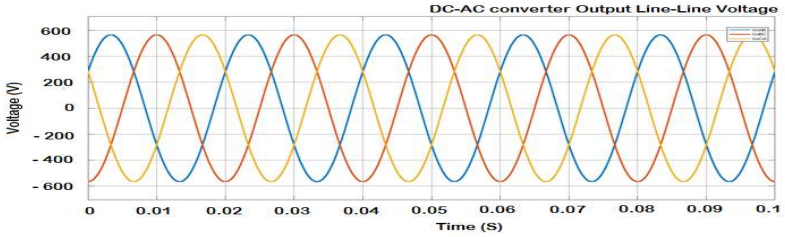


Fig. 8: Output line to line voltage of the DC-AC converter

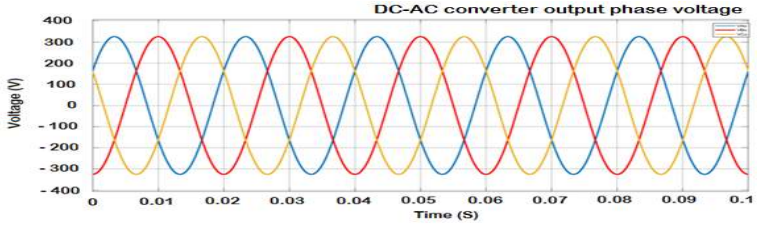


Fig. 9: Output phase voltage of the DC-AC converter

THD of the DC-AC converter was obtained to be 1.23% as presented in Fig.10. This value was well within the IEEE 519, 2012 THD standard limits.

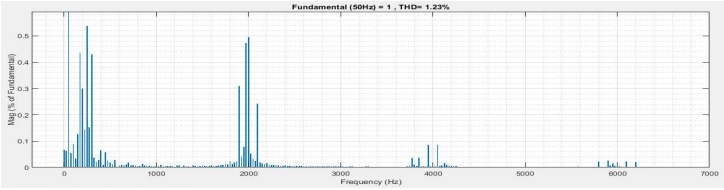


Fig. 10: DC-AC converter FFT analysis result

5. CONCLUSION

A three phase DC-AC active converter has been designed. The converter design was achieved with a reduced THD that corroborate to the IEEE 519, 2012 THD standard limit. The achievement was as a result of use of three phase LCL filter to further mitigate harmonics and SVPWM that provided more efficient control.

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